"El saber de mis hijos hará mi grandeza"

Back-End-of-Line 3D Integration Using Memristors and Thin-Fim Transistors for Next-Generation Silicon Circuits

Dr. Norberto Hernández Como
Contact: nohernandezc@ipn.mx
Instituto Politécnico Nacional, México.

The continual scaling and performance enhancement of silicon-based integrated circuits have motivated the exploration of innovative three-dimensional (3D) integration techniques. This work investigates the integration of memristors and thin-film transistors (TFTs) within the back-end-of-line (BEOL) layers of silicon transistor technology as a promising approach to achieving compact, high-density 3D architectures. By leveraging the unique memory and switching characteristics of memristors coupled with the low-temperature fabrication and compatibility of TFTs, this approach aims to enhance device functionality, improve circuit performance, and reduce the interconnect delays inherent in traditional planar designs. The study presents fabrication strategies, electrical characterization, and potential applications in artificial neural networks, neuromorphic computing, Dynamic Random-Access Memory (DRAM) and advanced logic circuits, highlighting the advantages and challenges of BEOL 3D integration using these emerging devices.

In 2006, he earned his bachelor's degree in electronic engineering with a major in Communications from the Oaxaca Institute of Technology. In 2012, he earned his Ph.D. in Electrical Engineering from the Center for Research and Advanced Studies of the Instituto Politécnico Nacional (CINVESTAV-IPN), focusing on the development of crystalline silicon/amorphous silicon heterojunction solar cells. He joined the University of Texas at Dallas (UTD) as a Research Associate in the Natural Science and Engineering Research Laboratory, leading the operation of pulsed laser deposition (PLD) and cryogenic Hall effect characterization systems. His work at UTD focused on the fabrication of thin-film transistors, diodes, solar cells, and photodetectors based on II-VI compounds. Since 2013, he has been working at the Centro de Nanociencias y Micro y Nanotecnologías at IPN, where he specializes in cleanroom-based semiconductor device and integrated circuit fabrication and testing made of emerging materials. He is a National System of Researchers (SNI) Level II member and a Senior Member of IEEE. Over his career, he has published over 40 articles in international journals and supervised more than 20 undergraduate, master's, and Ph.D. students.